University of California Riverside

EE/CS120A – Logic Design – 2021 Fall

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Homework 2

**Problem 1:** Manipulate a circuit in Figure 1 so that it uses only NAND gates

Diagram

Description automatically generated

Solution:

Diagram

Description automatically generated

**Problem 2:** Using Karnaugh Maps, find a simplest SOP expression for each of the following functions.

1)

2)

3)

1. Solution

K-Map

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | X’Y’ | X’Y | XY | XY’ |
| W’ | 0 | 1 | 1 | 0 |
| W | 0 | 1 | 1 | 1 |

This yields:

2. Solution

K-Map

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Y’Z’ | Y’Z | YZ | YZ’ |
| W’X’ | 1 | 1 | 0 | 0 |
| W’X | 0 | 0 | 1 | 1 |
| WX | 0 | 0 | 1 | 1 |
| WX’ | 1 | 1 | 0 | 0 |

This yields:

3. Solution

We know

K-Map

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | X’Y’ | X’Y | XY | XY’ |
| W’ | 1 | 0 | 1 | 1 |
| W | 0 | 0 | 0 | 0 |

This yields:

**Problem 3:** Using Karnaugh Maps, find the simplest POS expression for each of the following functions.

1)

2)

1. Solution

K-Map

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Y’Z’ | Y’Z | YZ | YZ’ |
| W’X’ | 1 | 1 | 0 | 0 |
| W’X | 0 | 0 | 1 | 1 |
| WX | 0 | 0 | 1 | 1 |
| WX’ | 1 | 1 | 0 | 0 |

To find the simplest POS

2. Solution

**Problem 4:** Sketch the outputs (Q and QN) of an SR-Latch (the basic latch) of the type shown in Figure 4 for the input waveforms shown below in Figure 4. Assuming that initially Q = 0 and QN = 1.

Diagram

Description automatically generated

**Problem 5:** Sketch the Output of a D Flip-flop for the input waveforms shown below. Assuming that initially Output = 0.

Diagram

Description automatically generated